Scholars Journal of Engineering and Technology (SJET) **ISSN 2321-435X (Online)**
Sch. J. Eng. Tech., 2014; 2(1):68-72 **ISSN 2347-9523 (Print)**

(An International Publisher for Academic and Scientific Resources)
www.saspublisher.com

Research Article

Low Power and High Speed Multiplexer Based Adder

Vimal Kant Pandey, Rajeev Kumar
Assistant Professor, DIT, Dehradun, India

***Corresponding author**
Vimal Kant Pandey
Email: vimalpandey94@gmail.com

Abstract: Full adder is a basic building block of many application specific integrated circuits. The paper evaluates and compares the performance of various full adder circuits which are designed using techniques such as XOR, transmission gates, multiplexers etc. Also a full adder circuit designed using multiplexer is proposed. The performance of these circuits is based on 180nm process model at supply voltage of 2.5V. The TSPICE simulation results show that the proposed circuit's performance is better as compare to the circuits that are found in literature whose performance is evaluated.
Keywords: XOR, power, full adder, transmission gate, multiplexer

INTRODUCTION

Most of the VLSI applications, such as digital-signal processing, data processing system and microprocessors use arithmetic operations extensively. The arithmetic unit is thus, heart of all these systems. Addition, subtraction, multiplication, and multiply and accumulate (MAC) are examples of the most commonly used operations of the arithmetic circuit. Binary addition is considered the most crucial part of the arithmetic unit because all other arithmetic operations usually involve addition [1, 2]. It is also a very critical operation because it involves a carry propagation step. The evaluation time of addition depends on the length of the operands .

Thus, the full adder which is the basic building block of all digital VLSI circuits should have been undergoes a considerable improvement, being motivated by three basic design goals, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed. The growth of portable devices like PDAs, cell phones, etc, demand high speed processing capabilities that also consume less power.The1-bit full adder is the building block of these operation modules. Thus, enhancing its performance is critical for enhancing the overall module performance. In this paper, we reviewed different i-bit full adder cells and also present a 1-bit full-adder cell using XOR gate with minimum transistor count and multiplex circuit that offers faster operation, and consumes less power than the other proposed full-adder cell found in the literature.

The rest of the paper is organized as follows: In section II, some standard implementations of the full adder circuits are discussed. In section III, the proposed design of 1-bit full adder based on the XOR-multiplexer circuit is presented. In section IV, simulation results for proposed and existing designs full adder circuits are given and comparisons are carried out with graph.

Prevoius Work

M. Vesterbacka *et al.* [3], the 16 transistor full adder circuits is designed using 6T XOR-XNOR circuit, one CMOS inverter and a multiplexer as shown in fig. 1. So, the circuit has a low device count, and also has full voltage- swing. Author also proposed another full adder circuit having 14 transistors as shown in Figure 2 .The circuit is composed of cross coupled pMOSFET and complementary cross coupled nMOSFET. These structures do not provide an output for A= B = 0 and A = B = 1, respectively, which is provided by the feedback of nMOSFET and pMOSFET marked with asterisks (*) in fig. 2.

D. Wang, M. Yang *et al.* [4], the 1 bit full adder circuit is designed using 3T XOR, 3T XNOR gate and two multiplexer as shown in fig. 3, the C input signal, which has full voltage swing and no extra delay, is used to drive the multiplexers, thereby reducing the overall delay.

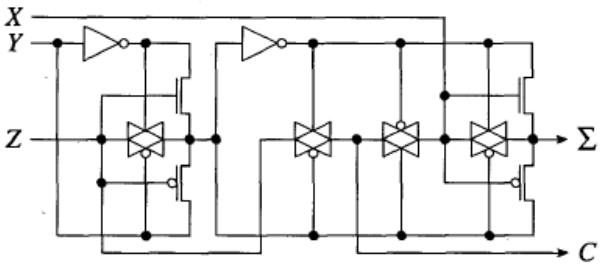

Fig. 1: 16-Transistor full adder circuit

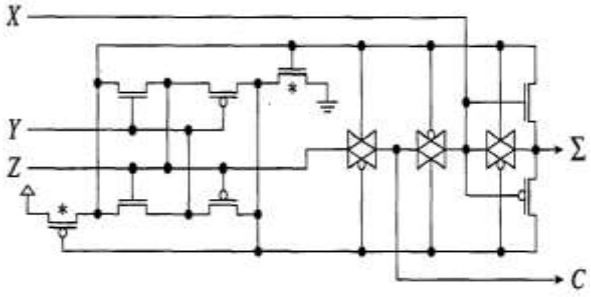

Fig. 2: 14-Transistor full adder circuit

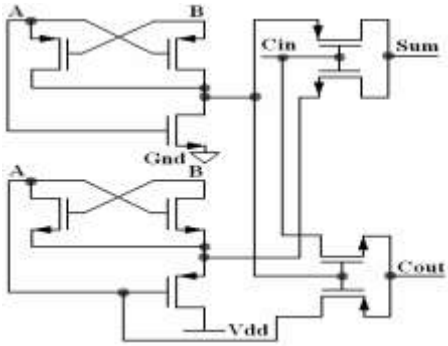

Fig. 3: 10-Transistor full adder circuit

Proposed Full Adder

The general mathematical equations for the "sum" and "carry" are given below in equations (1) and (2). The proposed designed circuit is the shown in the below given fig. 4:

$$SUM = A \oplus B \oplus Cin \quad (1)$$

$$Cout = (A \oplus B)Cin + AB \quad (2)$$

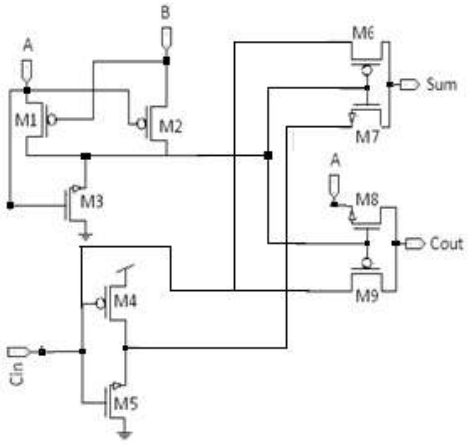

Fig. 4: Proposed full adder circuit

In the proposed circuit the transistor M1, M2 and M3 formed a XOR gate; M6 & M7 and M8 & M9 forms the multiplexers. The XOR gate provides the $A \oplus B$ operation and the outputs of XOR gate is

used as a select line to the two multiplexers which provides sum and carry respectively. The feature size of NMOS and PMOS in the XOR gate is used in such a way that it will give the correct output for all logic combinations. The operation of the circuit for different inputs is shown in table 1.

Table 1: The operation of the circuit for different inputs

INPUT			**ON/OFF TRANSISTOR**									**OUTPUT**	
A	B	C	M1	M2	M3	M4	M5	M6	M7	M8	M9	SUM	Cout
0	0	0	ON	ON	OFF	ON	OFF	ON	OFF	OFF	ON	0	0
0	0	1	ON	ON	OFF	ON	OFF	OFF	ON	OFF	ON	1	0
0	1	0	OFF	ON	OFF	OFF	ON	ON	OFF	ON	OFF	1	0
0	1	1	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF	0	1
1	0	0	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF	1	0
1	0	1	ON	OFF	ON	OFF	ON	OFF	0N	ON	OFF	0	1
1	1	0	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	ON	0	1
1	1	1	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	1	1

SIMULATION RESULTS

All the simulations have been done on TSPICE and all the schematics are designed on 180nm technology and simulation is done using power supply of 2.5V. The circuits are compared in terms of delay, power consumption and power delay product. The below given table 2 and 3 respectively gives the simulation results of different adder cells given in literature as well the proposed adder cell.

Table2: Rise, fall time, power and power delay product of SUM

Full Adder	**Raising Time***	**Falling Time***	**Propagation delay***	**Power***	**PDP&**
16T	20.18	30.19	25.18	55.41	1395.22
14T	20.22	29.88	25.05	55.57	1392.02
10T	27.82	19.50	23.66	45.80	1083.62
9T	0.008	0.014	0.011	42.32	.4655
Units- *=ns,&=ns x ns					

Table 3: Rise, fall time, power and power delay product of CARRY

Full Adder	Raising Time*	Falling Time*	Propagation delay*	Power*	PDP&
16T	60.35	40.05	50.20	55.21	1664.58
14T	60.15	39.73	49.94	55.57	2775.16
10T	66.52	40.03	53.27	45.80	2439.99
9T	.3116	.3228	.3172	42.32	13.42
Units- *=ns,&=ns x ns					

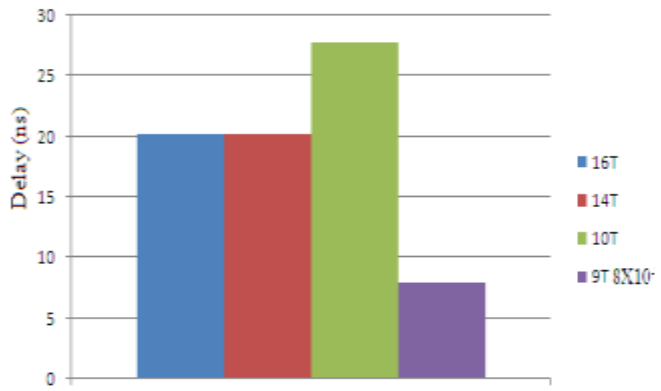

Fig. 5: Comparison of delay Rising Time for Sum

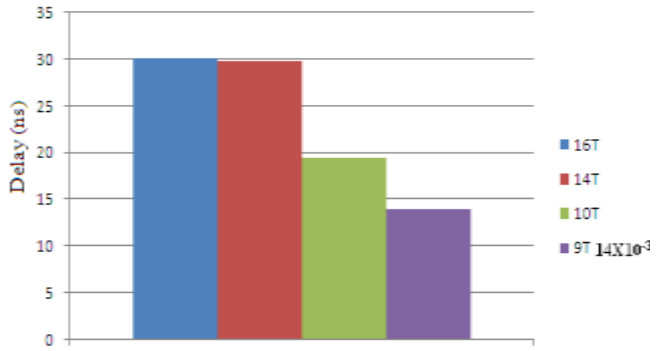

Fig. 6: Comparison of delay Falling Time for Sum

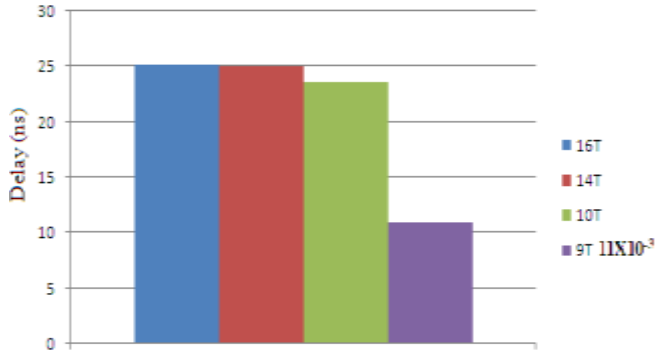

Fig. 7: Comparison of Propagation Delay for Sum

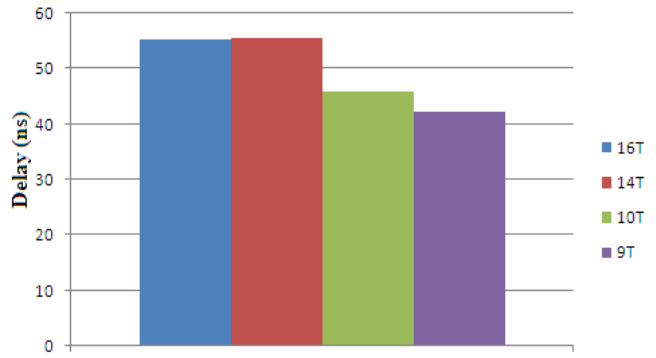

Figure.8. Comparison of Power Consumption for Sum & Carry

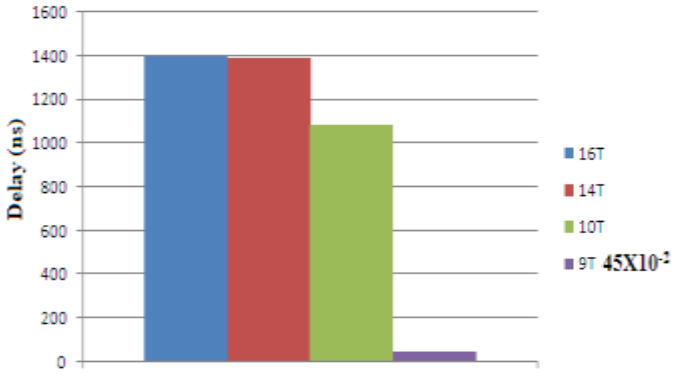

Figure.9. Comparison of PDP for Sum

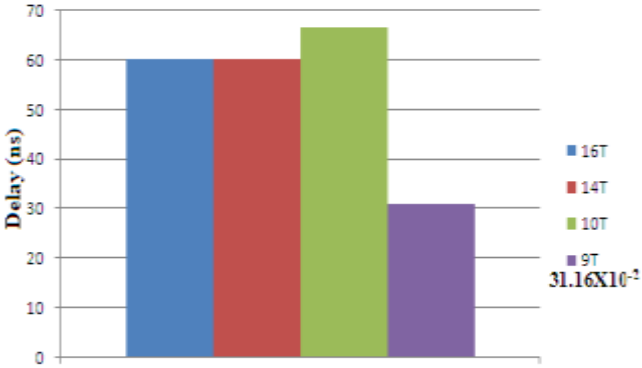

Figure.10. Comparison of delay Rising Time for Carry

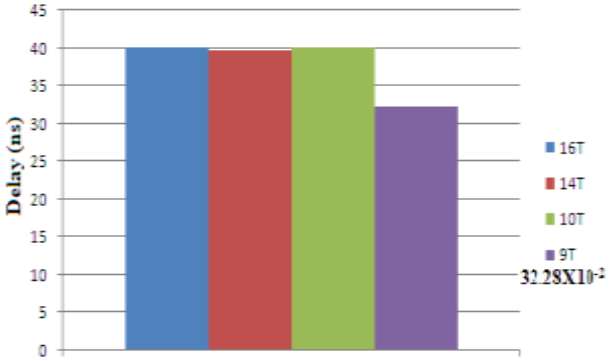

Figure.11. Comparison of delay Falling Time for Carry

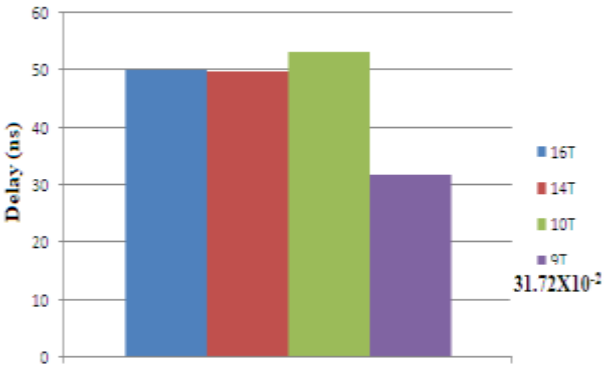

Figure.12. Comparison of Propagation Delay for Carry

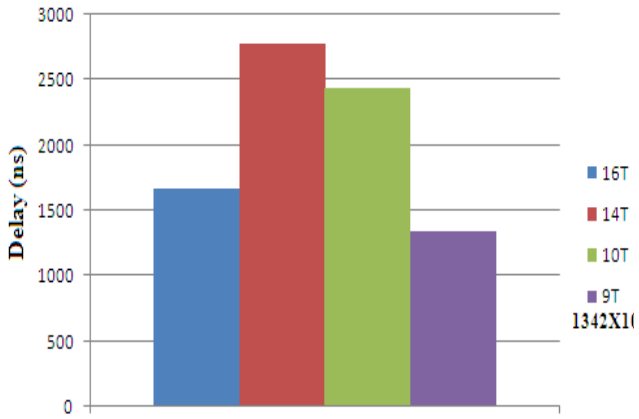

Figure.13. Comparison of PDP for Carry

CONCLUSION

In this paper, performance of three adder cells is compared by the proposed adder cell which is designed by using XOR and multiplexer. The simulation results show that the proposed adder is efficient in terms of delay, power consumption and power delay product.

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